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How to configure BCM53134 SGMII Port Speed through SPI or MDC/MDIO

Summary
This article describes how to configure BCM53134 B0/B1 chip SGMII port speed through SPI or MDC/MDIO interface.
It requires registers write to configure BCM53134 B0/B1 SGMII port speed on IMP Port State Override Register (0x00: 0x0e) for IMP port and STS_OVERRIDE_P5 Register (0x00: 0x5d) for Port5 and SerDes PHY register.

Description
Fo BCM53134B0/B1 chip

1. If OTP field sgmii_dis = 1, no SGMII interface support.
2. If OTP field sgmii_dis = 0, the strap pin SGMII_P8_SEL which shared with pin LED6 selects whether the SGMII interface gests multiplexed connected to Port 5 or Port 8.
   Since SGMII interface supports 1Gbps and up to 2.5Gbps, it requires the following registers setting to configure SGMII interface in 1Gbps or 2.5Gbps.
   - **Port 5**:
     Set STS_OVERRIDE_P5 Register (0x00: 0x5d) bit[3:2]=0x10 for 1000Mbps or 2500Mbps operation
   - **IMP port**:
     Set IMP Port State Override Register (0x00: 0x0e) bit[3:2]=0x10 for 1000Mbps or 2500Mbps operation
   - **SerDes PHY register**:
     - Configure SGMII as 1000BASE-X, the following registers programming sequence through SPI or MDC/MDIO interface access must to use.

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SPI Access		MDC/MDIO Pseudo PHY Access		Length	Byte1	Byte0
Page(SPI)	Offset(SPI)	MDIO Address	Offset(MDIO)			
0xe6	0x00	0xe6	0x00	0x1		0x01
0x14	0x3e	0x04	0x1f	0x2	0x80	0x00
0x14	0x20	0x04	0x10	0x2	0x0c	0x2f
0x14	0x3e	0x04	0x1f	0x2	0x83	0x00
0x14	0x20	0x04	0x10	0x2	0x01	0x0d
0x14	0x3e	0x04	0x1f	0x2	0x84	0x70
0x14	0x26	0x04	0x13	0x2	0x12	0x51
0x14	0x3e	0x04	0x1f	0x2	0x83	0x40
0x14	0x34	0x04	0x1a	0x2	0x00	0x03
0x14	0x3e	0x04	0x1f	0x2	0x80	0x00
0x14	0x00	0x04	0x00	0x2	0x01	0x40
0x14	0x20	0x04	0x10	0x2	0x2c	0x2f

- Configure SGMII as 2500BASE-X, the following registers programming sequence through SPI or MDC/MDIO interface access must to use.

SPI Access		MDC/MDIO Pseudo PHY Access		Length	Byte1	Byte0
Page(SPI)	Offset(SPI)	MDIO Address	Offset(MDIO)			
0xe6	0x00	0xe6	0x00	0x1		0x01
0x14	0x3e	0x04	0x1f	0x2	0x80	0x00
0x14	0x20	0x04	0x10	0x2	0x0c	0x2f
0x14	0x3e	0x04	0x1f	0x2	0x83	0x00
0x14	0x20	0x04	0x10	0x2	0x01	0x0d
0x14	0x30	0x04	0x18	0x2	0xc0	0x10
0x14	0x3e	0x04	0x1f	0x2	0x83	0x40
0x14	0x34	0x04	0x1a	0x2	0x00	0x01
0x14	0x3e	0x04	0x1f	0x2	0x80	0x00
0x14	0x00	0x04	0x00	0x2	0x01	0x40
0x14	0x20	0x04	0x10	0x2	0x2c	0x2f

- **SGMII Interface Speed Status**:
  There is SGMII Status Register (0xe6: 0x40) to double check the SGMII interface speed configure status.

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SGMII_STATUS

Register Address: SPI Page 0xe6, SPI Offset 0x40

Register Description: SGMII Status Register

Table 1294: SGMII_STATUS

Bits	Name	R/W	Description	Default
31:21	RESERVED	rw	Reserved	0x0
20:12	Reserved	ro	Reserved	0
11	PLL_LOCK	rw	PLL lock indication	0
10	SYM_ALGN	rw	Symbol alignment	0
9	SPD_2P5G	rw	2.5G Speed	0
8	SPD_1G	rw	1G Speed	0
7	SPD_100M	rw	100M Speed	0
6	SPD_10M	rw	10M Speed	0
5	SGMII_MODE	rw	SGMII Mode	0
4	RX_ALGN	rw	Rx bit alignment	0
3	RX_SIG_DET	rw	RX signal detect	0
2	TXP	rw	Tx Pause	0
1	RXP	rw	Rx Pause	0
0	LNK_STAT	rw	Link status	0